Abstract of the Disclosure

A device and method for providing inter-processor communication in a multi-processor architecture. A post office RAM has a plurality of mailboxes. Each mailbox is write-accessible by one port, but is read-accessible by the other ports. Thus, a processor device on a port has write-access to one mailbox, but can read the other mailboxes in the post office. A transmitting processor communicates with a receiving processor, by utilizing the post office. The transmitting processor writes information into its own mailbox, and signals a receiving processor. The receiving processor determines which of the processor devices signalled it, and reads the information in the transmitting processor's mailbox.